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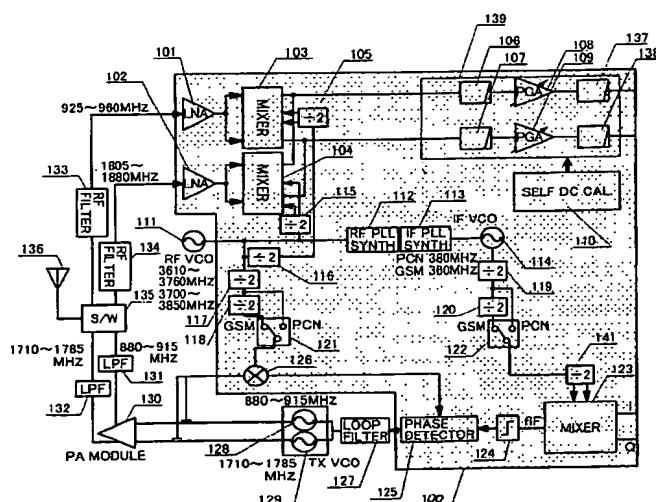
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(54) Multiband mobile communication apparatus

(57) A transceiver suitable for larger scale of integration employs direct conversion reception for reducing the number of filters. Also, the number of VCOs is reduced by utilizing dividers (105, 115, 116, 119, 120, 141) to supply a receiver and a transmitter with locally oscillated signals at an RF band. Dividers (105, 115, 116) each having a fixed division ratio are used for generating locally oscillated signals for the receiver, while a

divider (119, 120, 141) having a switchable division ratio are used for generating the locally oscillated signal for the transmitter. In addition, a variable gain amplifier (108) for baseband signal is provided with a DC offset voltage detector and a DC offset canceling circuit (110) for supporting high speed data communications to accomplish fast cancellation of a DC offset by eliminating intervention of a filter within a feedback loop for offset cancellation.

FIG.1



EP 1 102 413 A2

Description**BACKGROUND OF THE INVENTION****Field of the Invention**

[0001] The present invention relates generally to a mobile communication apparatus which can be implemented with a less number of components, and more particularly, to a transceiver which employs a direct conversion scheme suitable for larger scale of integration.

Description of the Related Art

[0002] With explosive popularization of mobile communication apparatus, requirements for a reduction in size and cost have been increased. For this reason, it is desired to eliminate VCO (voltage controlled oscillator), reduce the number of filters, and apply integrated circuits with a higher degree of integration. A prior art example of a transceiver which meets such requirements is described in K. Takikawa et. al., "RF Circuits Technique of Dual-Band Transceiver IC for GSM and DCS1800 applications," IEEE 25th European Solid-State Circuits Conference Preprints pp. 278-281, 1999. The configuration of this transceiver is illustrated in Fig. 10A. The illustrated transceiver comprises an integrated circuit 1016, and other components 1001 - 1015 which are connected external to the integrated circuit 1016. The prior art example supports two frequency bands, i. e., 900 MHz band and 1.8 GHz band. Also, the transceiver employs a superheterodyne scheme for a receiver and an offset PLL scheme for a transmitter. The superheterodyne receiver requires two RF (high frequency) filters 1001, 1002 for suppressing out-of-band blocker signals; two image rejection filters 1003, 1004 for rejecting blocker signals in an image frequency band associated with mixing; and an IF (intermediate frequency) filter 1005 for filtering out blocker signals near a reception channel. The receiver also requires two local oscillators 1006, 1007 for supporting the two frequency bands, i.e., 900 MHz band and 1.8 GHz band.

[0003] A reception scheme which can reduce the number of externally connected components is a direct conversion scheme. A prior art example of a direct conversion receiver is described in Behzad Razavi, "A 900-MHz CMOS Direct Conversion Receiver," IEEE Symposium on VLSI Circuits, pp. 113-114, 1997. The configuration of this receiver is illustrated in Fig. 10B. Since no image response exists in principle, the direct conversion scheme does not require an image rejection filter. Also, an IF filter is eliminated since it can be replaced by a filter integrated in an IC. In this prior art example, a VCO 1025 oscillates at a frequency twice an input frequency of the receiver which is in a range of 1850 - 1920 MHz. When this receiver is applied to GSM, DCS1800 dual band receiver, the VCO 1025 must oscillate in a range of 1850 to 1920 MHz (for GSM) and in

a range of 3610 to 3760 MHz (for DCS1800). However, since it is difficult for a single VCO to cover these frequency bands, two VCOs are required.

[0004] A widely known drawback of the direct conversion receiver is a DC offset voltage. This is generated because an input signal to mixers 1019, 1020 is equal to a locally oscillated signal in frequency. For example, if the locally oscillated signal leaks into an input terminal for an input signal, locally oscillated signals are mutually multiplied to generate DC offset voltage. A prior art example of a scheme for canceling the DC offset voltage is described in Asad A. Abidi et. al., "Direct-Conversion Radio Transceivers for Digital Communications," IEEE Journal of Solid-State Circuits, pp. 1399-1410, vol. 30, no. 12, Dec. 1995. The configuration of this transceiver is illustrated in Fig. 11. An output DC offset voltage of a variable gain amplifier composed of variable gain amplifiers 1101, 1103, 1105 and low pass filters 1102, 1104 is detected by a digital signal processor (DSP) 1106. The DSP 1106 outputs a DC offset voltage cancel signal to an input of the variable gain amplifier 1101 based on the detected information.

SUMMARY OF THE INVENTION

[0005] As described above, in the direct conversion receiver, the number of externally connected filters can be reduced. However, if the direct conversion receiver is used in place of the superheterodyne receiver in the GSM, DCS1800 dual band transceiver of Fig. 10A, the number of local oscillators is increased. This is because the transmitter requires a locally oscillated frequency in a range of 1150 to 1185 MHz (for GSM) and in a range of 1575 to 1650 MHz (for DCS1800), and the receiver requires a locally oscillated frequency in a range of 1850 to 1920 MHz (for GSM) and in a range of 3610 to 3760 MHz (for DCS1800), but a single VCO encounters difficulties in covering a plurality of bands. For a further reduction in cost, a reduction in the number of VCOs is a primary subject.

[0006] Also, in GPRS (General Packet Radio Service) which implements high speed data communications based on a GSM system, a plurality of slots are assigned to reception and transmission. Thus, fast DC offset voltage cancellation is required. In addition, the DC offset voltage cancellation must be performed every operation frame. First, the necessity for the fast offset cancellation is explained with reference to Fig. 4. One frame of GSM is comprised of eight slots, each of which has a duration of 577 μ s. Assume herein a severe condition for the DC offset voltage cancellation, in which four slots are assigned to the reception (RX), and one slot is assigned to the transmission (TX). While a transmission slot TX1' is assigned to a slot 7, the transmission slot TX1' is transmitted at a timing of TX1, which is 237 μ sec before the slot 7, in consideration of a propagation delay to a base station. Also, a monitoring period of approximately 500 μ sec and a PLL synchronizing period are required

other than transmission and reception. Assuming that the PLL synchronizing period lasts approximately 150 μ sec, a time available for canceling the DC offset voltage, in which a transceiver does not operate, is calculated as $1154-500-237-150*2=117$ μ sec, thus requiring fast DC offset cancellation.

[0007] Next, the necessity for the offset cancellation performed every frame is explained with reference to Fig. 5. Fig. 5 shows a measuring circuit for measuring a received frequency dependency of an output DC offset voltage of a mixer, and the result of a measurement made thereby. The result of the measurement reveals that the output DC offset voltage has the frequency dependency. Therefore, in a system such as GSM, DCS1800, in which a received frequency is not fixed during a call but the frequency hops within a reception band, it is difficult to previously anticipate the DC offset voltage. Therefore, the DC offset voltage must be canceled every operation frame.

[0008] The scheme employed in the example of Fig. 11 is not suitable for high speed data communications since a filter intervening in a feedback loop for offset cancellation make the fast offset cancellation difficult. Therefore, the realization of a fast offset canceling scheme suitable for high speed data communications is a second subject.

[0009] To realize the first subject, in the present invention, a receiver and a transmitter are supplied with locally oscillated signals in an RF band from a single VCO utilizing dividers. Dividers each having a fixed division ratio are used for generating the locally oscillated signals for the receiver, while a divider having a switchable division ratio is used for generating the locally oscillated signal for the transmitter.

[0010] To realize the second subject, in the present invention, a variable gain amplifier for baseband signal is provided with a DC offset voltage detector and a DC offset canceling circuit to accomplish fast cancellation of a DC offset by eliminating intervention of a filter within a feedback loop for offset cancellation.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011]

Fig. 1 is a block diagram illustrating the configuration of a mobile communication apparatus according to a first embodiment of the present invention; Fig. 2 is a block diagram illustrating a receiver of the mobile communication apparatus according to the present invention; Fig. 3 is a circuit diagram illustrating in detail a circuit for removing a DC offset of a receiver according to the present invention; Fig. 4 is an operation timing diagram in a GSM standard; Fig. 5 shows a method of measuring a DC offset voltage generated by a mixer, and the result of a

measurement made by the method;

Figs. 6A, 6B, 6C are diagrams illustrating the principles of the operation of a chopper amplifier which can be applied to the present invention;

5 Fig. 7 is a block diagram illustrating an embodiment in which a chopper amplifier is applied to the receiver of the present invention;

10 Fig. 8 is a block diagram illustrating a circuit for canceling a DC offset voltage for a variable gain amplifier without influence of a previous circuit in the receiver of the present invention;

15 Fig. 9 is a block diagram showing that a timing signal for removing a DC offset can be provided from a baseband circuit;

20 Fig. 10A is a block diagram illustrating the configuration of a mobile communication apparatus to which a conventional superheterodyne scheme is applied;

25 Fig. 10B is a block diagram illustrating the configuration of a prior art direct conversion receiver;

Fig. 11 shows a prior art DC offset voltage canceling technique;

30 Fig. 12 is a table showing IF frequencies of a transmitter for use in a GSM operation;

Fig. 13 is a table showing IF frequencies of the transmitter for use in a DCS1800 operation;

Fig. 14 shows a method of decoupling a filter capacitance to accelerate a DC offset removing operation;

35 Fig. 15 shows a method of decoupling a filter capacitance to simplify a DC offset removing circuit;

Fig. 16 is a block diagram illustrating a GSM/DCS1800 dual band transmitter;

40 Fig. 17 is a table listing spurious in GSM transmission;

Fig. 18 is a table listing spurious in DCS1800 transmission;

45 Fig. 19 shows a GSM spurious standard;

Fig. 20 shows allocation of VCO oscillating frequencies in which locally oscillated frequency bands are coincident for transmission and reception;

Fig. 21 shows allocation of VCO oscillating frequencies in which locally oscillated frequency bands do not overlap for transmission and reception;

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0012] A first embodiment of the present invention will be described with reference to Fig. 1. The first embodiment uses an exemplary mobile communication apparatus, as an application, which supports the European cellular telephone GSM (900 MHz band) and DCS1800 (1800 MHz band).

[0013] A direct conversion scheme is applied to a receiver for converting an RF signal directly to a baseband signal, and the offset PLL scheme, previously shown in the prior art example, is applied to a transmitter. The receiver comprises low noise amplifiers 101, 102; mix-

ers 103, 104; and a variable gain low pass filter 139. Each of the mixers converts a signal frequency band from the RF band to the baseband, and simultaneously performs demodulation for separating an RF signal into a sine component and a cosine component. For this purpose, the mixers 103, 104 must be applied with locally oscillated signals which are shifted in phase by 90°. The locally oscillated signals are generated using dividers 105, 115. The locally oscillated signals are generated by a PLL loop formed of a VCO 111 and a PLL 112. When a VCO for oscillating in a 3600 MHz band is used for the VCO 111, the output of the divider 115 is in a 1800 MHz band and provides a locally oscillated signal for DCS1800. Also, as the divider 116 is positioned prior to the divider 105, an output frequency of the divider 105 is in a 900 MHz band and provides a locally oscillated signal for GSM. Output baseband signals of the mixers 103, 104 are inputted to a variable gain low pass filter 139 for level adjustment and blocker signal rejection. The variable gain low pass filter 139 comprises low pass filters 106, 107, 137, 138, and variable gain amplifiers 108, 109. Also, for suppressing a DC offset voltage at the output of the variable gain low pass filter 139, a DC offset voltage canceling circuit 110 is provided. The DC offset voltage canceling circuit 110 has a DC offset voltage detecting unit and a DC offset canceling unit.

[0014] For reducing the number of externally connected components, the transmitter also uses the same VCO 111 as the receiver. How to determine an IF frequency (fIF) used in the transmitter is explained below. Assume that reception frequencies received at an antenna 136 are f_{rG} (for GSM) and f_{rD} (for DCS1800); and a transmission frequencies are f_{tG} (for GSM) and f_{tD} (for DCS1800). As described above, since the oscillating frequency of the VCO 111 is four times the GSM reception frequency and twice the DSC1800 reception frequency, the oscillating frequency of the VCO 111 can be expressed as $4 \cdot f_{rG} = 2 \cdot f_{rD}$. When signals generated by dividing this oscillating frequency by m (GMS) and by n (DCS1800) are used as locally oscillated signals for a mixer 126 of an offset PLL, an IF frequency fIF_G for GSM is expressed by the following equation 1:

$$fIF_G = \left| \frac{4 \cdot f_{rG}}{m} - f_{tG} \right| \quad \text{equation 1}$$

[0015] Similarly, an IF frequency fIF_D for DCS1800 is expressed by the following equation 2:

$$fIF_D = \left| \frac{2 \cdot f_{rD}}{n} - f_{tD} \right| \quad \text{equation 2}$$

[0016] Assume herein that $f_{rG}=925$ MHz, $f_{tG}=880$ MHz, $f_{rD}=1805$ MHz, and $f_{tD}=1710$ MHz. The IF frequency fIF_G calculated for m is shown in Fig. 12, and the IF frequency fIF_D calculated for n is shown in Fig.

13. Since a divide-by-two divider is used for the frequency division, 2 to the i -th power (i is an integer number) is used for m and n . For employing a single VCO for generating the IF frequencies, m and n cannot be freely selected but must be selected such that fIF_G is substantially equal to fIF_D . Also, when a divide-by-two divider is used, the ratio of fIF_G to fIF_D may be substantially equal to 2 to the j -th power (j is an integer number). Here, "substantially equal" means that the two frequencies may be included within an oscillating frequency range of the VCO even if they are not exactly the same. In Figs. 12 and 13, combinations of m and n which satisfy the foregoing condition are $(m, n) = (2, 1)$ and $(4, 2)$. The IF frequencies fIF are eventually determined from such combinations of m and n in consideration of power consumption, the presence or absence of generation of an unwanted spurious signal, and so on. In this embodiment, a combination $(m, n) = (4, 2)$ is chosen. Dividers 117, 118 and a change-over switch 121 are provided subsequent to the VCO 111, and are controlled to divide the output frequency of VCO 111 by four for GSM and by two for DCS1800. Next, the oscillating frequency of the VCO 114 is determined depending on the power consumption, the scale of passive elements contained in IC, and so on. In this embodiment, the oscillating frequency of the VCO 114 is divided by eight for GSM and by four for DCS1800 to generate $fIF_G=45$ MHz and $fIF_D=95$ MHz by selecting the oscillating frequency in a 300 MHz band and providing dividers 119, 120 and a change-over switch 122 subsequent to the VCO 114.

[0017] Next, the problem of spurious will be explained in a more specific manner. Figs. 17, 18 show the spurious when the IF frequency is fixed, and the locally oscillated frequency is changed. Figs. 17, 18, which correspond to GSM and DSC1800, show the spurious which results from the difference between an integer multiple (multiplied by m) of the IF frequency and the locally oscillated frequency when transmission signals are generated from transmission oscillators 128, 124. In the tables, fIF represents the IF frequency, and $fVCO$ the transmission frequency. A numerical value written in each field shows the difference between a spurious signal and the transmission frequency in units of MHz. Hatched fields indicate the spurious generated nearby within 10 MHz, which are not easily removed by a loop filter 127 of the transmitter. As will be understood from Figs. 17, 18, when the IF frequency is fixed, it is difficult to avoid a region in which the spurious appears near the transmission frequency within the transmission band, and the effectiveness of varying the IF frequency depending on the transmission frequency is understandable. For example, in the example of GSM shown in Fig. 17, the spurious can be avoided by selecting the IF frequency at 45 MHz from 880 MHz to 888 MHz and selecting the IF frequency at 46 MHz from 888 MHz to 914 MHz.

[0018] In this embodiment, the locally oscillated signal applied to the mixer 126 in the transmitter exists within

the reception band. Fig. 16 illustrates the transmitter of this embodiment in an enlarged view. The locally oscillated signal existing within the reception band leaks through a path designated by 2309, and amplified by an amplifier at a later stage and irradiated. A standard related to the irradiation of the spurious in GSM is summarized in Fig. 19. While the spurious within the reception band is allowed only at five points and at a level of -36 dBm or lower, it is desired to suppress the spurious to -79 dBm/100kHz in principle. Fig. 20 summarizes the oscillating frequencies of the VCO so far explained in the foregoing embodiment. A reception band 2701 and a transmission band 2703 for DCS1800 are coincident, and a reception band 2702 and a transmission band 2704 for GSM are coincident as well. For shifting these bands from each other, consider a frequency allocation as shown in Fig. 21. A transmission band 2705 shifted from the reception band 2701 for DCS1800 does not overlap the reception band 2701, so that the leakage of the locally oscillated frequency within the reception band during transmission can be avoided. The same is applied to GSM as well.

[0019] Next, a receiver according to a second embodiment of the present invention will be described with reference to Fig. 2.

[0020] The illustrated receiver comprises a low noise amplifier 102; a mixer 104; a divider 105; low pass filters 106, 137; variable gain amplifiers 108, 201; DC offset voltage canceling circuits 110; and a decoder 205. The low noise amplifier 102 in turn comprises a load resistor 207; a transistor 208; and a capacitance 209, while the DC offset voltage canceling circuit 110 comprises a digital-to-analog converter (DAC) 202; an analog-to-digital converter (ADC) 203; and a controller 204. The mixer 104 comprises mixers 210, 206.

[0021] An output DC voltage of the variable gain amplifier 108 is converted to a digital signal by the ADC 203, and inputted to the controller 204. The controller 204 measures the DC offset voltage at the output of the variable gain amplifier 108 to output a cancel signal for canceling the DC offset voltage. The cancel signal is converted from a digital signal to an analog signal by the DAC 202, and an output signal of the DAC 202 cancels the DC offset voltage of the variable gain amplifier 108. The decoder 205 selects one of the DC offset voltage canceling circuits 110, such that only the selected circuit is operative. In this way, since no filter intervenes within a feedback loop comprised of the variable gain amplifier and the DC offset voltage canceling circuit, a delay otherwise caused by the filter is eliminated, thereby making it possible to realize fast offset cancellation. Here, it is also possible to employ a one-bit ADC, i.e., a simple comparator.

[0022] Next, a variable gain amplifier and a DC offset voltage canceling circuit according to a third embodiment of the present invention will be described with reference to Fig. 3.

[0023] The variable gain amplifier comprises resistors

307, 308, 312; and transistors 309, 310, 311. The transistors 309, 310 are applied with an input voltage at their bases to deliver output voltages from their collectors. The gain can be controlled, for example, by a base voltage 5 of the transistor 311. A DAC 313 comprises transistors 301, 302, 303; and resistors 304, 305, 306. Since the output of a controller 204 is connected to bases of the transistors 301, 302, 303, the controller 204 can control collector DC currents of the transistors 301, 302, 10 303. The collector DC currents are summed with a collector current of the transistor 309, and then converted to a voltage by the resistor 307. Assume now that a DC offset voltage $\Delta V (=V_2-V_1)$ exists, and the resistance of the resistors 307, 308 are represented by R_L ; an output DC current 15 of the DAC 313 by I_{DAC1} ; and an output DC current of the DAC 314 by I_{DAC2} . In this event, the controller 204 controls the DACs 313, 314 to satisfy the relationship expressed by equation 3:

$$R_L \cdot (I_{DAC1} - I_{DAC2}) = \Delta V \quad \text{equation 3}$$

[0024] Next, a variable gain amplifier according to a fourth embodiment of the present invention will be described with reference to Figs. 6A - 6C. Fig. 6A illustrates an ideal variable gain amplifier 603 free from a DC offset voltage, and an input conversion DC offset voltage source 606 for the variable gain amplifier 603. In this configuration, since no means is provided for suppressing an offset voltage, an output voltage of the offset voltage source 606 multiplied by the gain of the variable gain amplifier 603 appears as an offset between output terminals 604, 605. Next, Figs. 6B, 6C illustrate configurations in which change-over switches 607, 608, i.e., 25 the third embodiment according to the present invention, are connected to the input and output of the variable gain amplifier 603. Since Fig. 6B is opposite to Fig. 6C in the connection relationship of the change-over switches 607 and 608, an output voltage of the offset 30 voltage source 606 is transmitted to an opposite terminal, i.e., to 604 in Fig. 6B and to 605 in Fig. 6C, while maintaining the connection relationship between the input and output terminals. Therefore, when the aforementioned change-over switches 607, 608 are periodically 35 changed over, the output voltage of the offset voltage source 606 appears at the output terminals 604, 605 for the same time, so that the offset voltage between the output terminals becomes zero.

[0025] Next, a receiver according to a fifth embodiment of the present invention will be described with reference to Fig. 7. This embodiment shows a receiver characterized in that the variable gain amplifier 609 shown in the third embodiment is employed in place of the variable gain amplifier 201 and the DC offset voltage canceling circuit 206 in the second embodiment, and a low pass filter 702 and a buffer amplifier 701 are connected subsequent to the variable gain amplifier 609.

[0026] Next, a receiver according to a sixth embodiment of the present invention will be described with reference to Fig. 8. This embodiment shows a receiver characterized in that a switch 801 is connected between the low pass filter 140 and the variable gain amplifier 201 in the second embodiment. For canceling a DC offset voltage, the switch 801 is turned on to short-circuit inputs of the variable gain amplifier 201, and the switch 801 is maintained off when the cancellation is not performed. By turning on the switch 801 upon starting the cancellation, the variable gain amplifier 201 can perform the cancellation without being affected by a DC offset voltage from the previous stage.

[0027] Next, a mobile communication apparatus according to a seventh embodiment of the present invention will be described with reference to Fig. 9. This embodiment shows a mobile communication apparatus characterized in that a baseband circuit 901 is added to the first embodiment. A block 907 includes all circuits other than an antenna 139 and a circuit 143 contained in IC in the first embodiment. The baseband circuit 901 performs signal processing such as conversion of received baseband signals 902, 903 to audio signals, conversion of audio signals to transmission baseband signals 905, 906, and so on. Further, the baseband circuit 901 outputs a DC offset cancel starting signal 904 for determining the timing at which a DC offset voltage is canceled in the circuit 143, and inputs the signal 904 to the circuit 143. The starting signal is sent before a receiver starts receiving a signal, such that a DC offset generated in the circuit 143 is removed before receiving the signal.

[0028] Next, a mobile communication apparatus according to an eighth embodiment of the present invention will be described with reference to Fig. 14. Switches 1401, 1402 are inserted between a capacitance 1403 and resistors 1404, 1405 in a filter 140 to reduce the time constant during DC offset cancellation. Since this can reduce a propagation delay through the filter 140, the DC offset can be canceled faster without using the input short-circuiting switch 801 illustrated in Fig. 8. Also, when respective amplifiers 108, 201 are comprised of bipolar transistors as illustrated in Fig. 3, the bases of the transistors are biased through filter resistors 1404, 1405. Therefore, the DC offset voltage can be canceled, including a bias offset due to variations in base current and variations in filter resistor. On the other hand, the sixth embodiment employing the short-circuiting switch 801 cannot cancel the bias offset. In addition, when the DC offset is removed in order from former stages, a residual error is removed by the DC offset canceling function at a later stage, so that a more accurate DC offset removal can be achieved.

[0029] Next, a mobile communication apparatus according to a ninth embodiment of the present invention will be described with reference to Fig. 15. When a propagation delay through the filter is reduced as in the eighth embodiment, the filter can be interposed in a

feedback loop for canceling the DC offset voltage. Therefore, this embodiment can reduce the number of ADCs and accordingly the scale of the circuit, as compared with the eighth embodiment.

[0030] According to the present invention, three externally connected filters and one externally connected VCO can be saved as compared with the conventional superheterodyne receiver. In addition, it is possible to realize a mobile communication apparatus which can support a high speed packet transmission mode with a reduced number of parts by removing fast a DC offset voltage which causes a problem in the direct conversion receiver.

15
Claims

1. A transceiver comprising:

20 a receiver including a first voltage controlled oscillator (VCO) (111), first and second dividers (105, 115, 116) connected to an output of said first VCO (111), a first mixer (103) receiving an output signal of said first divider (105, 116) and a first RF signal, and a second mixer (104) receiving an output signal of said second divider (115) and a second RF signal; and
25 a transmitter including a third divider (117, 118), connected to the output of said first VCO (111), having means (121) for switching a first division ratio and a second division ratio, a second VCO (114), a fourth divider (119, 120, 141), connected to an output of said second VCO (114), having means (122) for switching a third division ratio and a fourth division ratio, a third mixer (123) receiving an output signal of said fourth divider (119, 120, 141) and a baseband signal, and a frequency conversion circuit (125, 126, 127, 128, 129) for converting the frequency of an output signal of said third mixer (123) using an output signal of said third divider (117, 118).

30 40 45 50 55 60 65 70 75 80 85 90 95 100 105 110 115 120 125 130 135 140 145 150 155 160 165 170 175 180 185 190 195 200 205 210 215 220 225 230 235 240 245 250 255 260 265 270 275 280 285 290 295 300 305 310 315 320 325 330 335 340 345 350 355 360 365 370 375 380 385 390 395 400 405 410 415 420 425 430 435 440 445 450 455 460 465 470 475 480 485 490 495 500 505 510 515 520 525 530 535 540 545 550 555 560 565 570 575 580 585 590 595 600 605 610 615 620 625 630 635 640 645 650 655 660 665 670 675 680 685 690 695 700 705 710 715 720 725 730 735 740 745 750 755 760 765 770 775 780 785 790 795 800 805 810 815 820 825 830 835 840 845 850 855 860 865 870 875 880 885 890 895 900 905 910 915 920 925 930 935 940 945 950 955 960 965 970 975 980 985 990 995 1000 1005 1010 1015 1020 1025 1030 1035 1040 1045 1050 1055 1060 1065 1070 1075 1080 1085 1090 1095 1100 1105 1110 1115 1120 1125 1130 1135 1140 1145 1150 1155 1160 1165 1170 1175 1180 1185 1190 1195 1200 1205 1210 1215 1220 1225 1230 1235 1240 1245 1250 1255 1260 1265 1270 1275 1280 1285 1290 1295 1300 1305 1310 1315 1320 1325 1330 1335 1340 1345 1350 1355 1360 1365 1370 1375 1380 1385 1390 1395 1400 1405 1410 1415 1420 1425 1430 1435 1440 1445 1450 1455 1460 1465 1470 1475 1480 1485 1490 1495 1500 1505 1510 1515 1520 1525 1530 1535 1540 1545 1550 1555 1560 1565 1570 1575 1580 1585 1590 1595 1600 1605 1610 1615 1620 1625 1630 1635 1640 1645 1650 1655 1660 1665 1670 1675 1680 1685 1690 1695 1700 1705 1710 1715 1720 1725 1730 1735 1740 1745 1750 1755 1760 1765 1770 1775 1780 1785 1790 1795 1800 1805 1810 1815 1820 1825 1830 1835 1840 1845 1850 1855 1860 1865 1870 1875 1880 1885 1890 1895 1900 1905 1910 1915 1920 1925 1930 1935 1940 1945 1950 1955 1960 1965 1970 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020 2025 2030 2035 2040 2045 2050 2055 2060 2065 2070 2075 2080 2085 2090 2095 2100 2105 2110 2115 2120 2125 2130 2135 2140 2145 2150 2155 2160 2165 2170 2175 2180 2185 2190 2195 2200 2205 2210 2215 2220 2225 2230 2235 2240 2245 2250 2255 2260 2265 2270 2275 2280 2285 2290 2295 2300 2305 2310 2315 2320 2325 2330 2335 2340 2345 2350 2355 2360 2365 2370 2375 2380 2385 2390 2395 2400 2405 2410 2415 2420 2425 2430 2435 2440 2445 2450 2455 2460 2465 2470 2475 2480 2485 2490 2495 2500 2505 2510 2515 2520 2525 2530 2535 2540 2545 2550 2555 2560 2565 2570 2575 2580 2585 2590 2595 2600 2605 2610 2615 2620 2625 2630 2635 2640 2645 2650 2655 2660 2665 2670 2675 2680 2685 2690 2695 2700 2705 2710 2715 2720 2725 2730 2735 2740 2745 2750 2755 2760 2765 2770 2775 2780 2785 2790 2795 2800 2805 2810 2815 2820 2825 2830 2835 2840 2845 2850 2855 2860 2865 2870 2875 2880 2885 2890 2895 2900 2905 2910 2915 2920 2925 2930 2935 2940 2945 2950 2955 2960 2965 2970 2975 2980 2985 2990 2995 3000 3005 3010 3015 3020 3025 3030 3035 3040 3045 3050 3055 3060 3065 3070 3075 3080 3085 3090 3095 3100 3105 3110 3115 3120 3125 3130 3135 3140 3145 3150 3155 3160 3165 3170 3175 3180 3185 3190 3195 3200 3205 3210 3215 3220 3225 3230 3235 3240 3245 3250 3255 3260 3265 3270 3275 3280 3285 3290 3295 3300 3305 3310 3315 3320 3325 3330 3335 3340 3345 3350 3355 3360 3365 3370 3375 3380 3385 3390 3395 3400 3405 3410 3415 3420 3425 3430 3435 3440 3445 3450 3455 3460 3465 3470 3475 3480 3485 3490 3495 3500 3505 3510 3515 3520 3525 3530 3535 3540 3545 3550 3555 3560 3565 3570 3575 3580 3585 3590 3595 3600 3605 3610 3615 3620 3625 3630 3635 3640 3645 3650 3655 3660 3665 3670 3675 3680 3685 3690 3695 3700 3705 3710 3715 3720 3725 3730 3735 3740 3745 3750 3755 3760 3765 3770 3775 3780 3785 3790 3795 3800 3805 3810 3815 3820 3825 3830 3835 3840 3845 3850 3855 3860 3865 3870 3875 3880 3885 3890 3895 3900 3905 3910 3915 3920 3925 3930 3935 3940 3945 3950 3955 3960 3965 3970 3975 3980 3985 3990 3995 4000 4005 4010 4015 4020 4025 4030 4035 4040 4045 4050 4055 4060 4065 4070 4075 4080 4085 4090 4095 4100 4105 4110 4115 4120 4125 4130 4135 4140 4145 4150 4155 4160 4165 4170 4175 4180 4185 4190 4195 4200 4205 4210 4215 4220 4225 4230 4235 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6240 6245 6250 6255 6260 6265 6270 6275 6280 6285 6290 6295 6300 6305 6310 6315 6320 6325 6330 6335 6340 6345 6350 6355 6360 6365 6370 6375 6380 6385 6390 6395 6400 6405 6410 6415 6420 6425 6430 6435 6440 6445 6450 6455 6460 6465 6470 6475 6480 6485 6490 6495 6500 6505 6510 6515 6520 6525 6530 6535 6540 6545 6550 6555 6560 6565 6570 6575 6580 6585 6590 6595 6600 6605 6610 6615 6620 6625 6630 6635 6640 6645 6650 6655 6660 6665 6670 6675 6680 6685 6690 6695 6700 6705 6710 6715 6720 6725 6730 6735 6740 6745 6750 6755 6760 6765 6770 6775 6780 6785 6790 6795 6800 6805 6810 6815 6820 6825 6830 6835 6840 6845 6850 6855 6860 6865 6870 6875 6880 6885 6890 6895 6900 6905 6910 6915 6920 6925 6930 6935 6940 6945 6950 6955 6960 6965 6970 6975 6980 6985 6990 6995 7000 7005 7010 7015 7020 7025 7030 7035 7040 7045 7050 7055 7060 7065 7070 7075 7080 7085 7090 7095 7100 7105 7110 7115 7120 7125 7130 7135 7140 7145 7150 7155 7160 7165 7170 7175 7180 7185 7190 7195 7200 7205 7210 7215 7220 7225 7230 7235 7240 7245 7250 7255 7260 7265 7270 7275 7280 7285 7290 7295 7300 7305 7310 7315 7320 7325 7330 7335 7340 7345 7350 7355 7360 7365 7370 7375 7380 7385 7390 7395 7400 7405 7410 7415 7420 7425 7430 7435 7440 7445 7450 7455 7460 7465 7470 7475 7480 7485 7490 7495 7500 7505 7510 7515 7520 7525 7530 7535 7540 7545 7550 7555 7560 7565 7570 7575 7580 7585 7590 7595 7600 7605 7610 7615 7620 7625 7630 7635 7640 7645 7650 7655 7660 7665 7670 7675 7680 7685 7690 7695 7700 7705 7710 7715 7720 7725 7730 7735 7740 7745 7750 7755 7760 7765 7770 7775 7780 7785 7790 7795 7800 7805 7810 7815 7820 7825 7830 7835 7840 7845 7850 7855 7860 7865 7870 7875 7880 7885 7890 7895 7900 7905 7910 7915 7920 7925 7930 7935 7940 7945 7950 7955 7960 7965 7970 7975 7980 7985 7990 7995 8000 8005 8010 8015 8020 8025 8030 8035 8040 8045 8050 8055 8060 8065 8070 8075 8080 8085 8090 8095 8100 8105 8110 8115 8120 8125 8130 8135 8140 8145 8150 8155 8160 8165 8170 8175 8180 8185 8190 8195 8200 8205 8210 8215 8220 8225 8230 8235 8240 8245 8250 8255 8260 8265 8270 8275 8280 8285 8290 8295 8300 8305 8310 8315 8320 8325 8330 8335 8340 8345 8350 8355 8360 8365 8370 8375 8380 8385 8390 8395 8400 8405 8410 8415 8420 8425 8430 8435 8440 8445 8450 8455 8460 8465 8470 8475 8480 8485 8490 8495 8500 8505 8510 8515 8520 8525 8530 8535 8540 8545 8550 8555 8560 8565 8570 8575 8580 8585 8590 8595 8600 8605 8610 8615 8620 8625 8630 8635 8640 8645 8650 8655 8660 8665 8670 8675 8680 8685 8690 8695 8700 8705 8710 8715 8720 8725 8730 8735 8740 8745 8750 8755 8760 8765 8770 8775 8780 8785 8790 8795 8800 8805 8810 8815 8820 8825 8830 8835 8840 8845 8850 8855 8860 8865 8870 8875 8880 8885 8890 8895 8900 8905 8910 8915 8920 8925 8930 8935 8940 8945 8950 8955 8960 8965 8970 8975 8980 8985 8990 8995 9000 9005 9010 9015 9020 9025 9030 9035 9040 9045 9050 9055 9060 9065 9070 9075 9080 9085 9090 9095 9100 9105 9110 9115 9120 9125 9130 9135 9140 9145 9150 9155 9160 9165 9170 9175 9180 9185 9190 9195 9200 9205 9210 9215 9220 9225 9230 9235 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- 126, 127, 128, 129).
4. A transceiver according to claim 3, wherein:
- 5 said frequency conversion circuit (125, 126, 127, 128, 129) comprises a phase comparator (125), a first low pass filter (127), third and fourth VCOs (128, 129), and a fourth mixer (126); and
- 10 said phase comparator (125) outputs a signal proportional to a difference in phase between an output signal of said third mixer (123) and an output signal of said fourth mixer (126), said first low pass filter (127) is connected to an output of said phase comparator (125), said third and fourth VCOs (128, 129) are connected to an output of said first low pass filter (127), and
- 15 said fourth mixer (126) is a mixer which includes a phase locked loop (PLL) for mixing an output signal of said third or fourth VCO (128, 129) with the output signal of said third divider (117, 118).
- 20 5. A transceiver comprising:
- 25 a variable gain low pass filter (139) receiving a baseband signal; and
- 30 an offset voltage canceling circuit (110) including means for canceling a DC offset voltage of said low pass filter,
- 35 said variable gain low pass filter (139) including a plurality of variable gain amplifiers (108, 109) and a plurality of low pass filters (106, 107, 137, 138).
- 40 6. A transceiver according to claim 5, wherein said offset voltage canceling circuit (110) comprises:
- 45 an analog-to-digital converter (ADC) (203) receiving an output signal of said variable gain amplifier;
- 50 a controller (204) for detecting a DC offset voltage of said variable gain amplifier from an output signal of said ADC (203) to output a signal for canceling said DC offset voltage; and
- 55 a digital-to-analog converter (DAC) (202) receiving the output signal of said controller (204) to output a signal to said variable gain amplifier.
- 60 7. A transceiver according to claim 6, wherein:
- 65 said variable gain amplifier comprises first and second transistors (309, 310) having their emitters connected to each other, a first resistor (307) connected to a collector of said first transistor (309) and a power supply, a second resistor (308) connected to a collector of said second transistor (310) and said power supply, and
- 70 a variable current source connected to said emitters, wherein a signal is inputted from bases of said first and second transistors (309, 310), and a signal is outputted from the collectors of said first and second transistors (309, 310); and
- 75 said DAC (202) comprises a plurality of voltage-to-current converters each including a third transistor (301, 302, 303) and a third resistor (304, 305, 306) connected to the emitter of said third transistor (304, 305, 306) and a ground, said third transistor (304, 305, 306) having a collector connected to the collector of said first transistor (309), and said third transistor (304, 305, 306) having a base connected to an output of said controller (204).
8. A transceiver according to claim 6, wherein:
- 80 said variable gain low pass filter (139) is configured of a differential circuit; and
- 85 said variable gain low pass filter (139) comprises a first switch (801) connected between first and second input terminals of at least one of said variable gain amplifiers, said first switch (801) being switched to a short-circuited state or to an open state through switching control.
9. A transceiver according to claim 6, wherein:
- 90 said variable gain low pass filter (139) is configured of a differential circuit, and at least one first low pass filter of said low pass filters includes second and third switches (1401, 1402) and a first capacitance (1403);
- 95 said second switch (1401) is connected to a first signal wire and said first capacitance (1403) of said first low pass filter, and said third switch (1402) is connected to a second signal wire and said first capacitance (1403) of said first low pass filter; and
- 100 said second and third switches (1401, 1402) are switched to a short-circuited state or to an open state in synchronism through switching control.
10. A transceiver according to claim 9, wherein:
- 105 said controller cancels a DC offset voltage of a first variable gain amplifier (108) connected in front of said first low pass filter, and comprises a first DAC (202) and a first controller (204), said first controller (204) being identical to a controller for canceling a DC offset voltage of a second variable gain amplifier (201) connected subsequent to said first low pass filter.
11. A transceiver according to claim 5, wherein:

said variable gain low pass filter (139) comprises a differential circuit; and
at least one of said variable gain amplifiers is replaced with a chopper type amplifier (609) having third and fourth input terminals and first and second output terminals; 5
said chopper type amplifier (609) includes a third variable gain amplifier (603) having fifth and sixth input terminals and third and fourth output terminals, a fourth switch (607), and a fifth switch (608); and
said fourth and fifth switches (607, 608) are controlled to switch between a first state in which said third input terminal is connected to said fifth input terminal; said fourth input terminal to said sixth input terminal; said first output terminal to said third output terminal; and said second output terminal to said fourth output terminal, and a second state in which said third input terminal is connected to said sixth input terminal; said fourth input terminal to said fifth input terminal; said first input terminal to said fourth output terminal; and said second output terminal to said third output terminal, said first and second states being periodically switched. 10
15
20
25

12. A mobile communication apparatus comprising:

an antenna (136);
an antenna switch (135) connected to said antenna (136); 30
a plurality of power amplifiers (130) for outputting signals to said antenna switch (135);
a plurality of bandpass filters (131, 132) connected to said antenna switch (135); and
a transceiver (100) connected to said bandpass filters (131, 132), said power amplifiers (130) and a baseband circuit (901), 35
said transceiver (100) being said transceiver according to claim 1; and
said baseband circuit (901) supplying said transceiver (100) with a signal for defining a timing at which a DC offset voltage canceling operation is started. 40
45

13. A mobile communication apparatus according to claim 12, wherein:

a duplexer is used in place of said antenna switch (135).

50

55

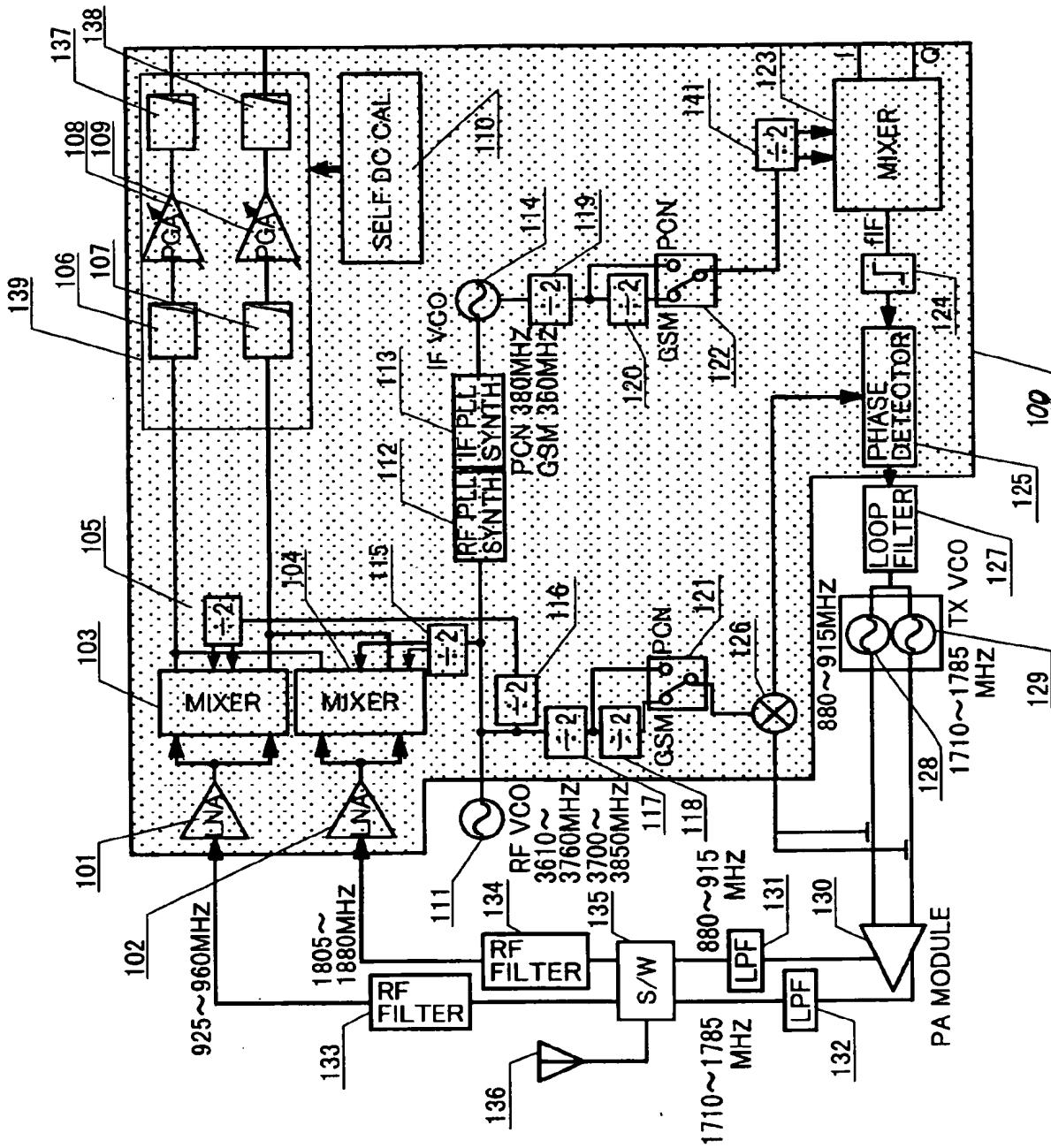


FIG. 1

FIG.2

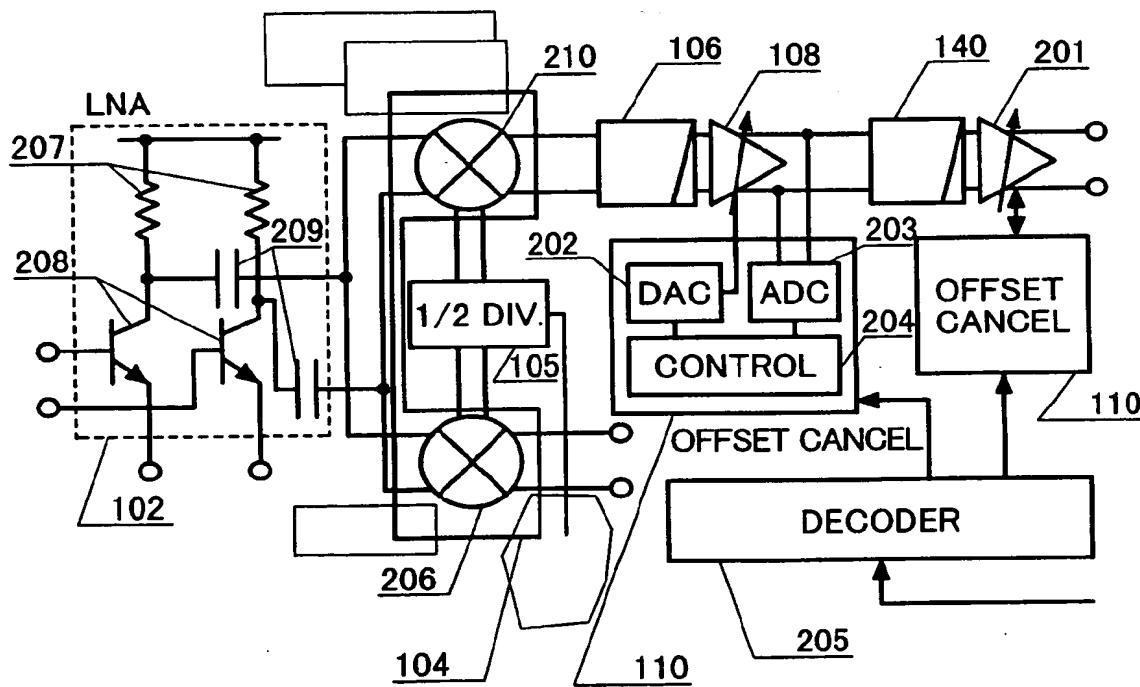


FIG.3

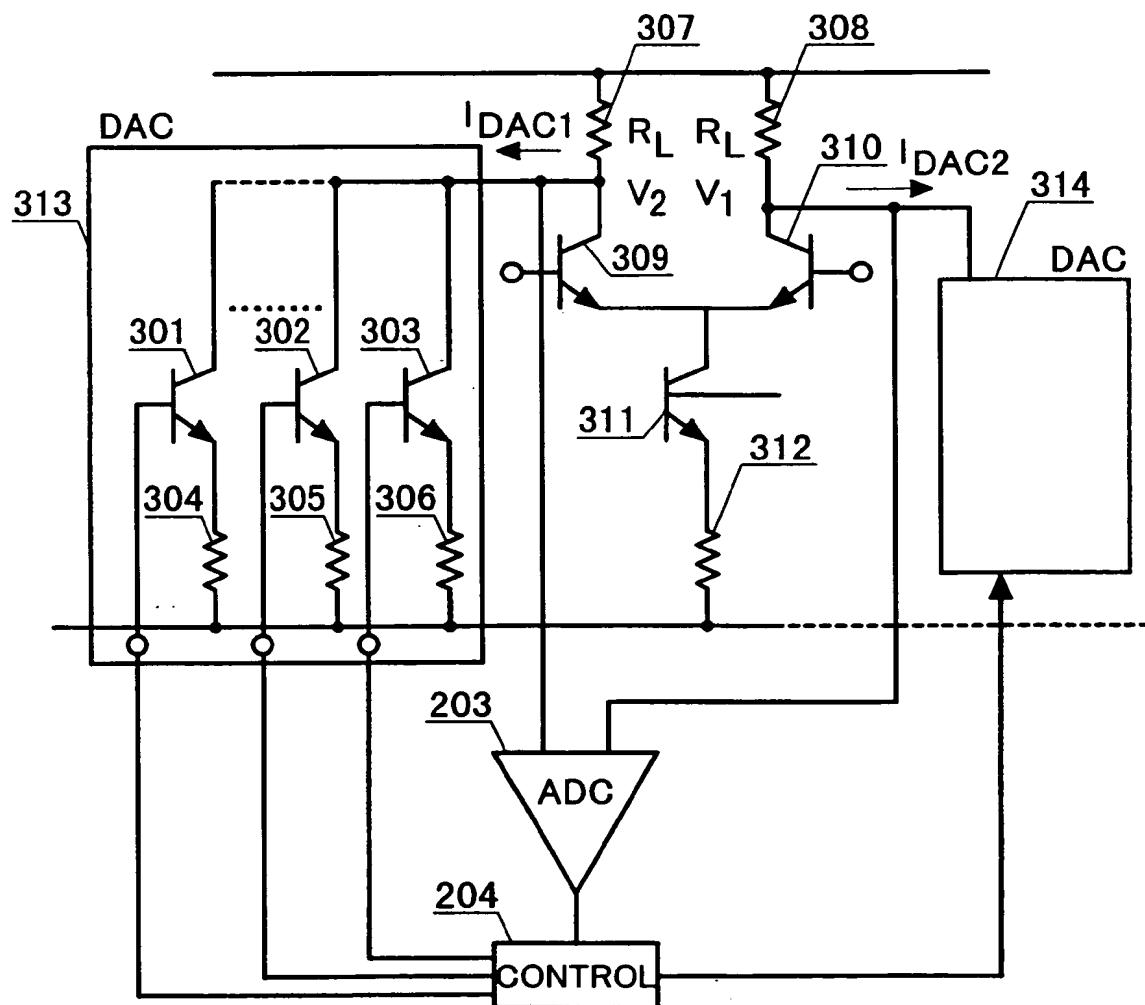


FIG.4

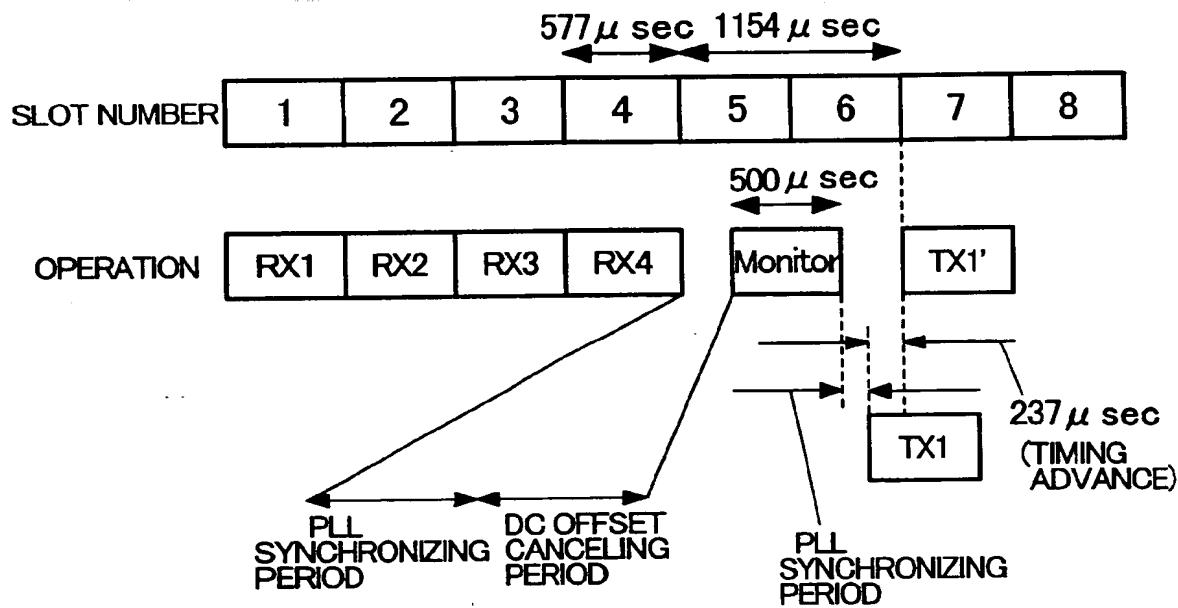


FIG.5

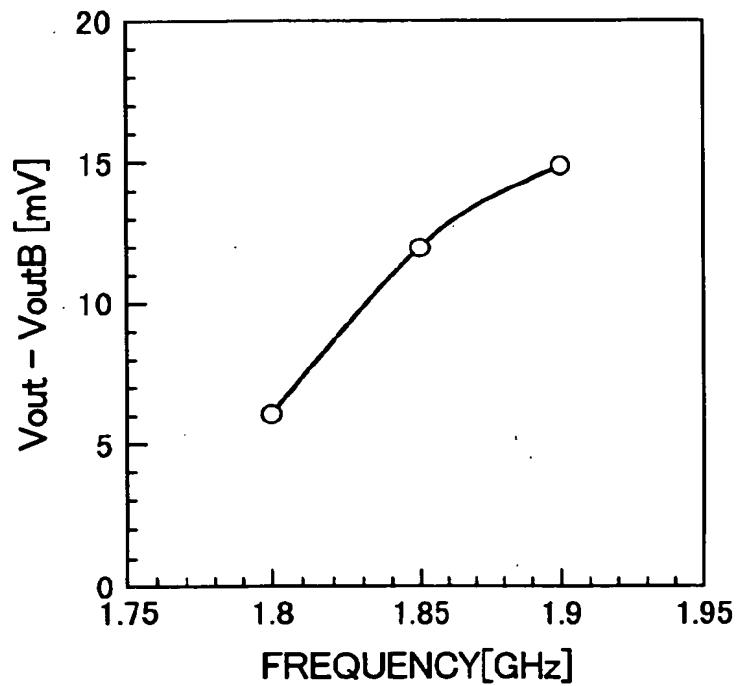
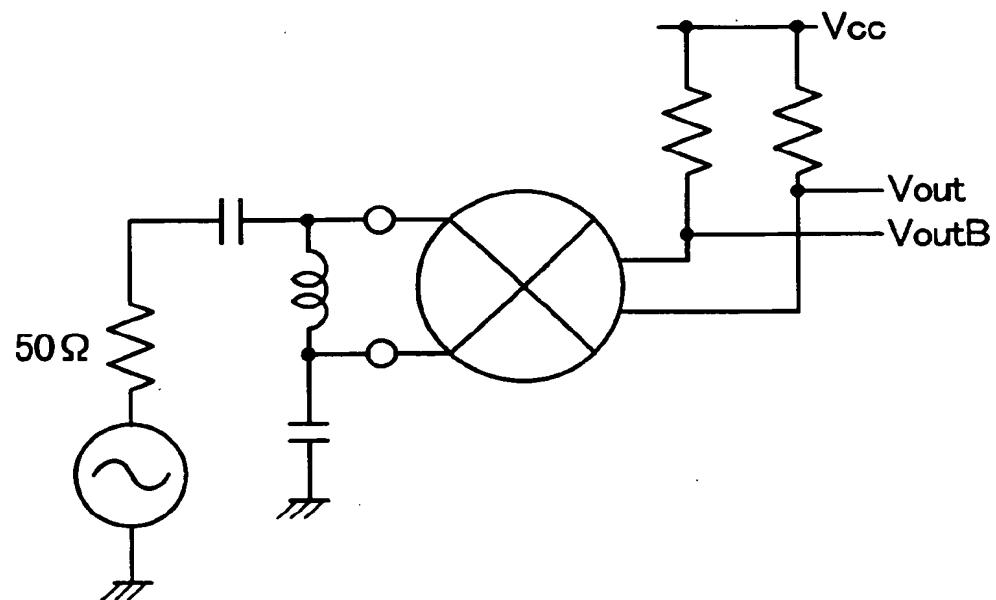


FIG.6A

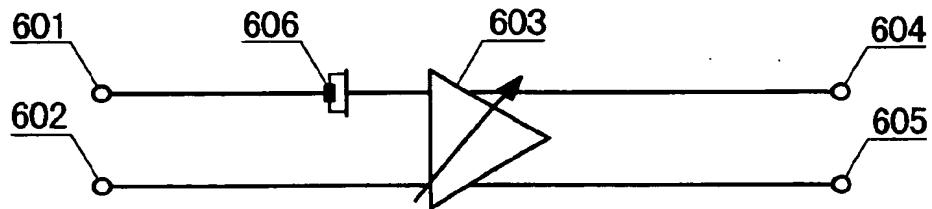


FIG.6B

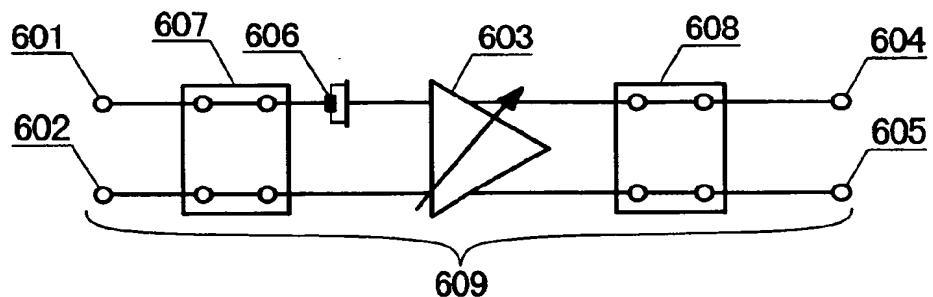


FIG.6C

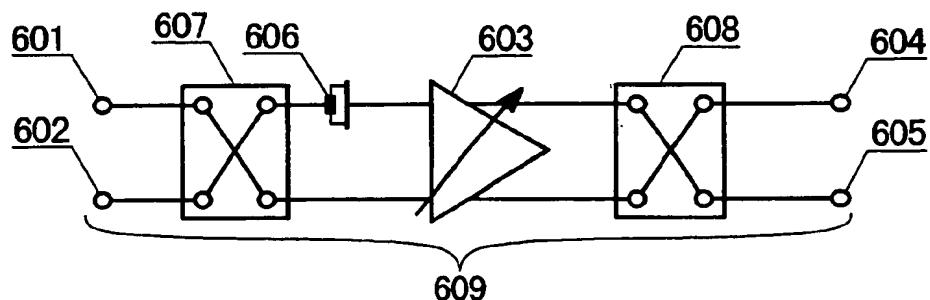


FIG.7

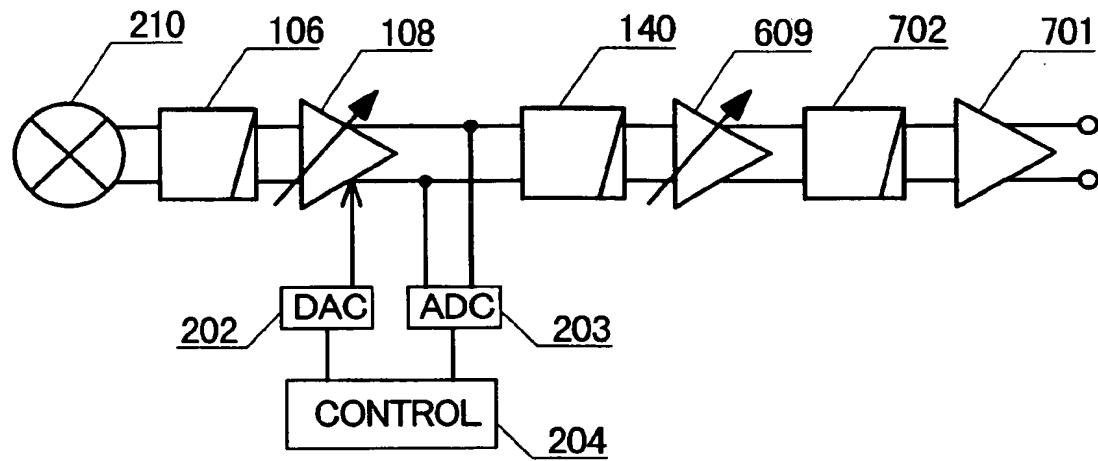


FIG.8

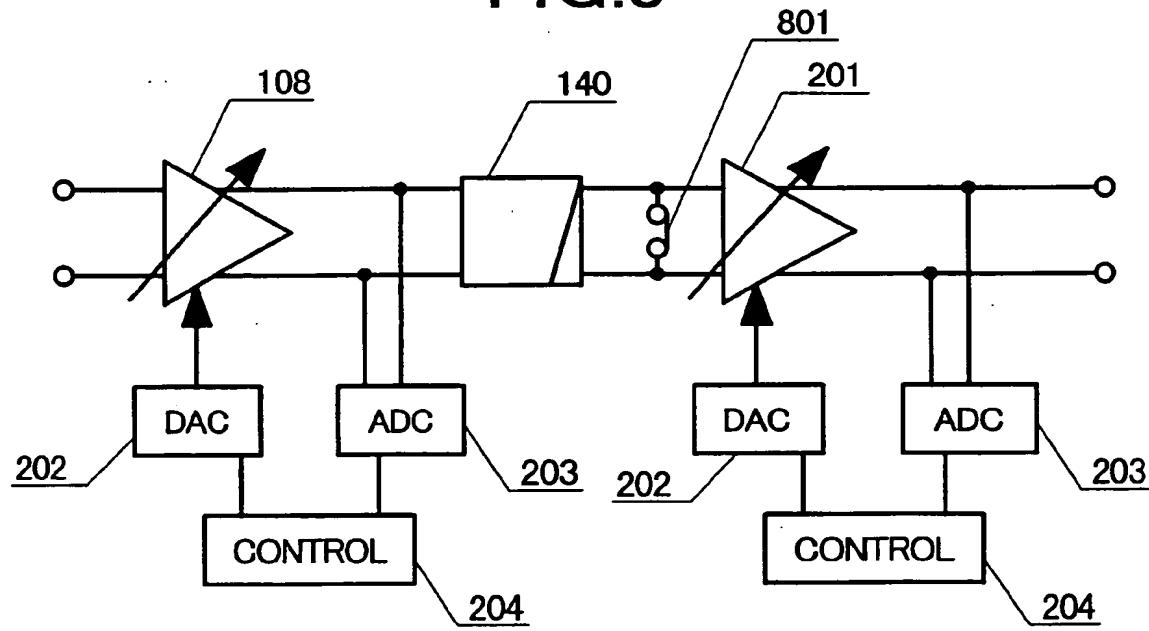


FIG.9

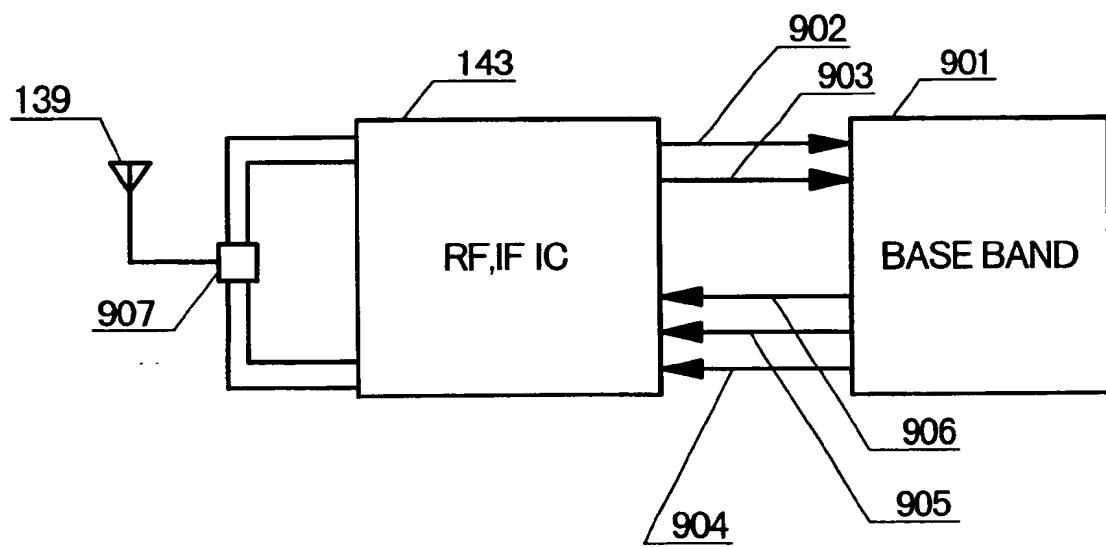


FIG. 10A

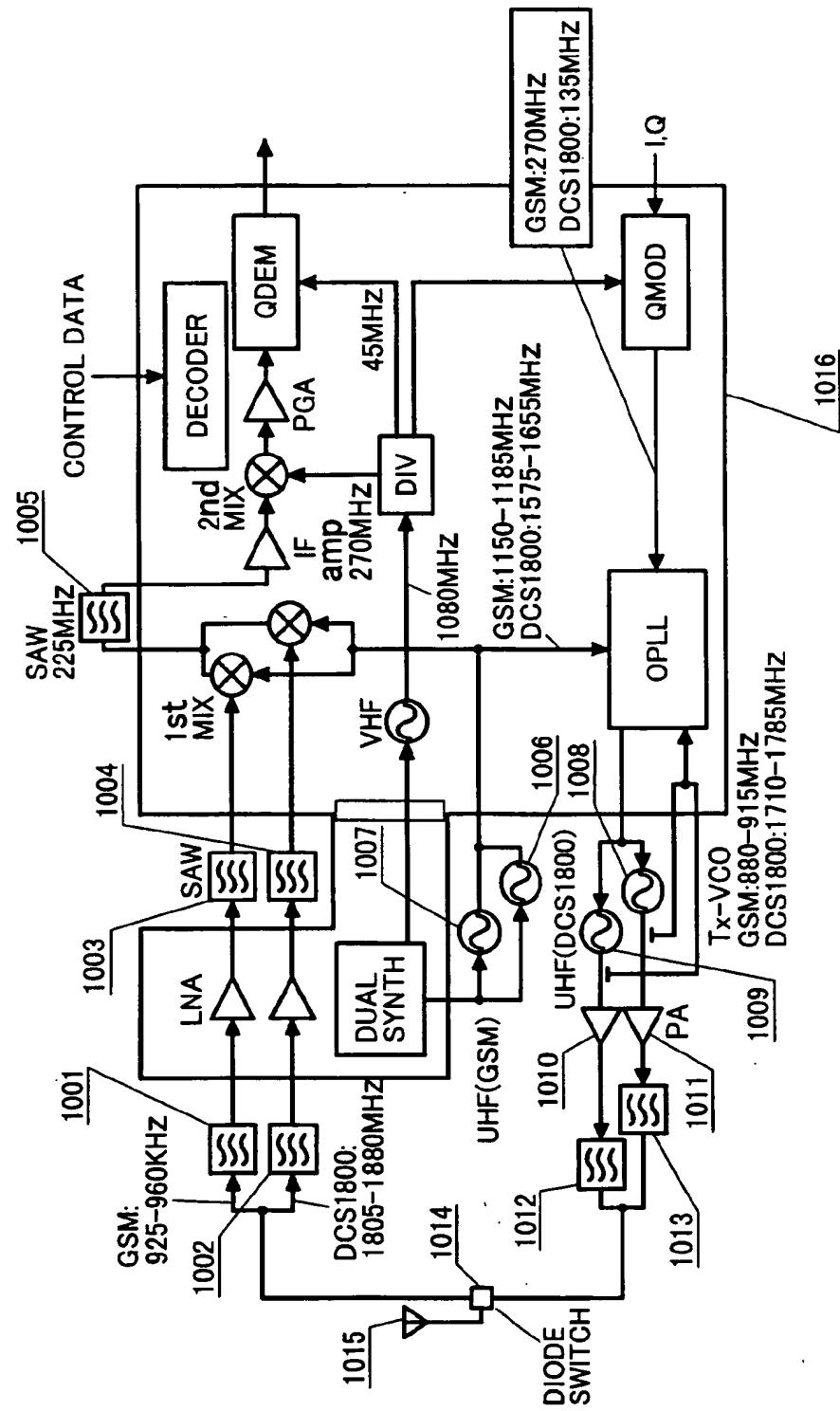


FIG.10B

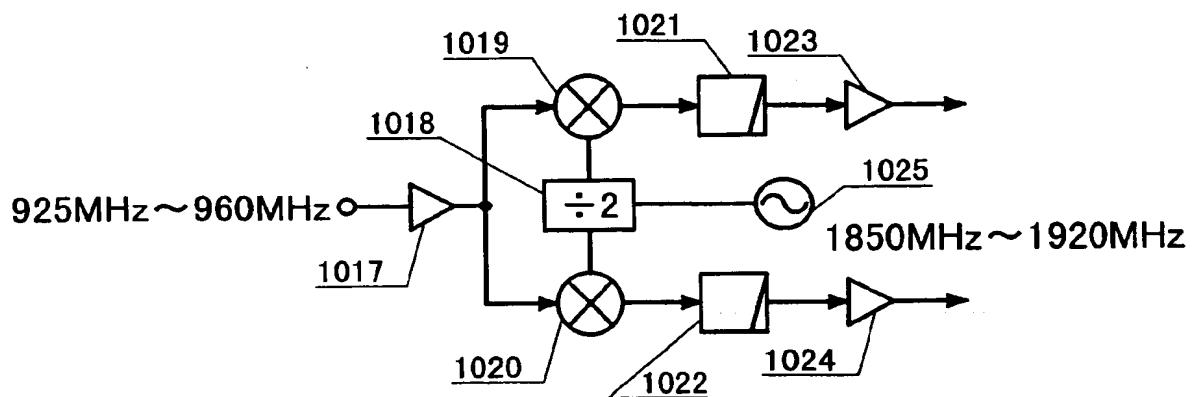


FIG.11

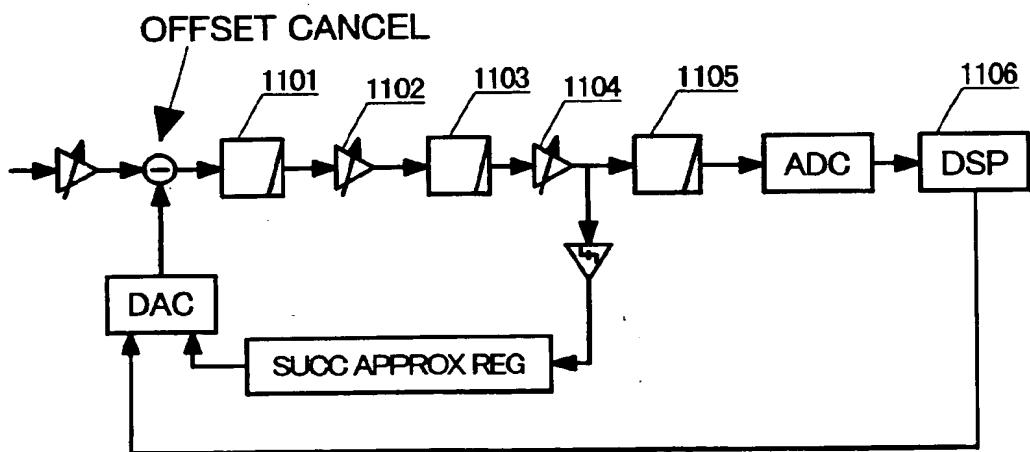


FIG.12

m	fIF_G [MHZ]
1	2820
2	970
4	45
8	417.5
16	648.75
32	764.375

FIG.13

n	fIF_D [MHZ]
1	1900
2	95
4	807.5
8	1258.75
16	1484.375
32	1597.1875

FIG.14

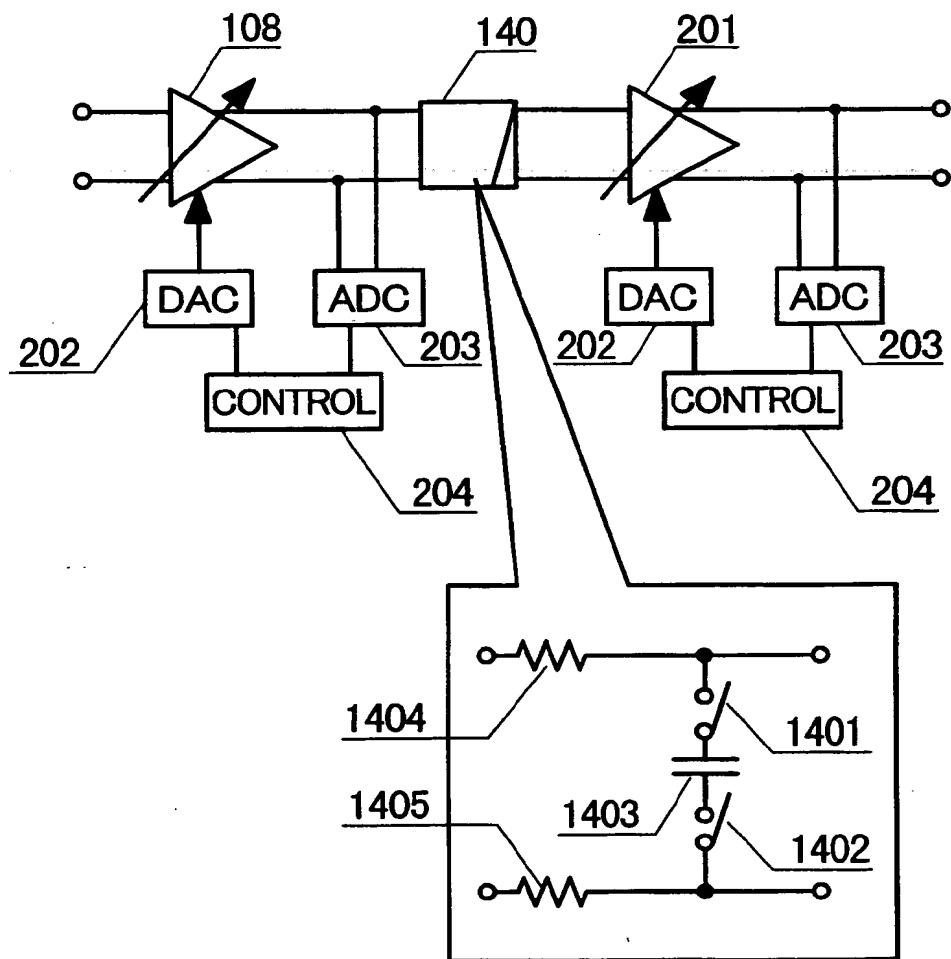


FIG.15

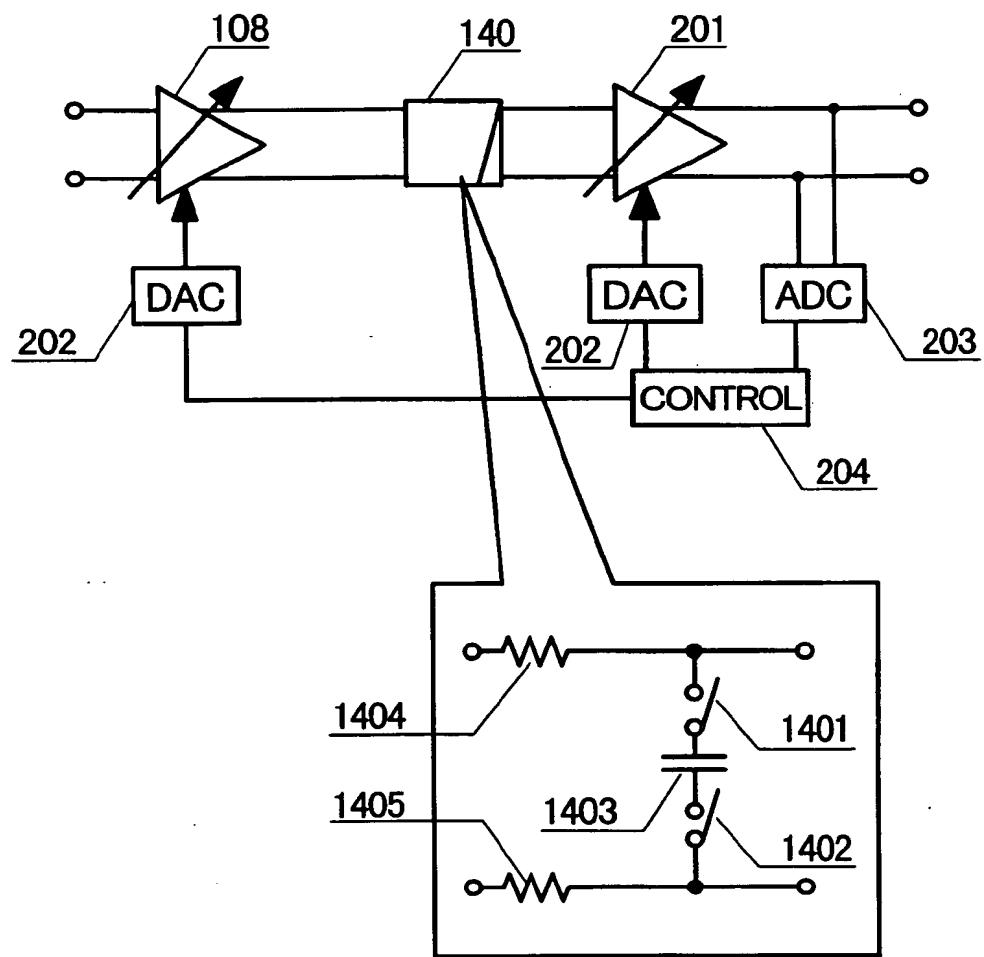


FIG.16

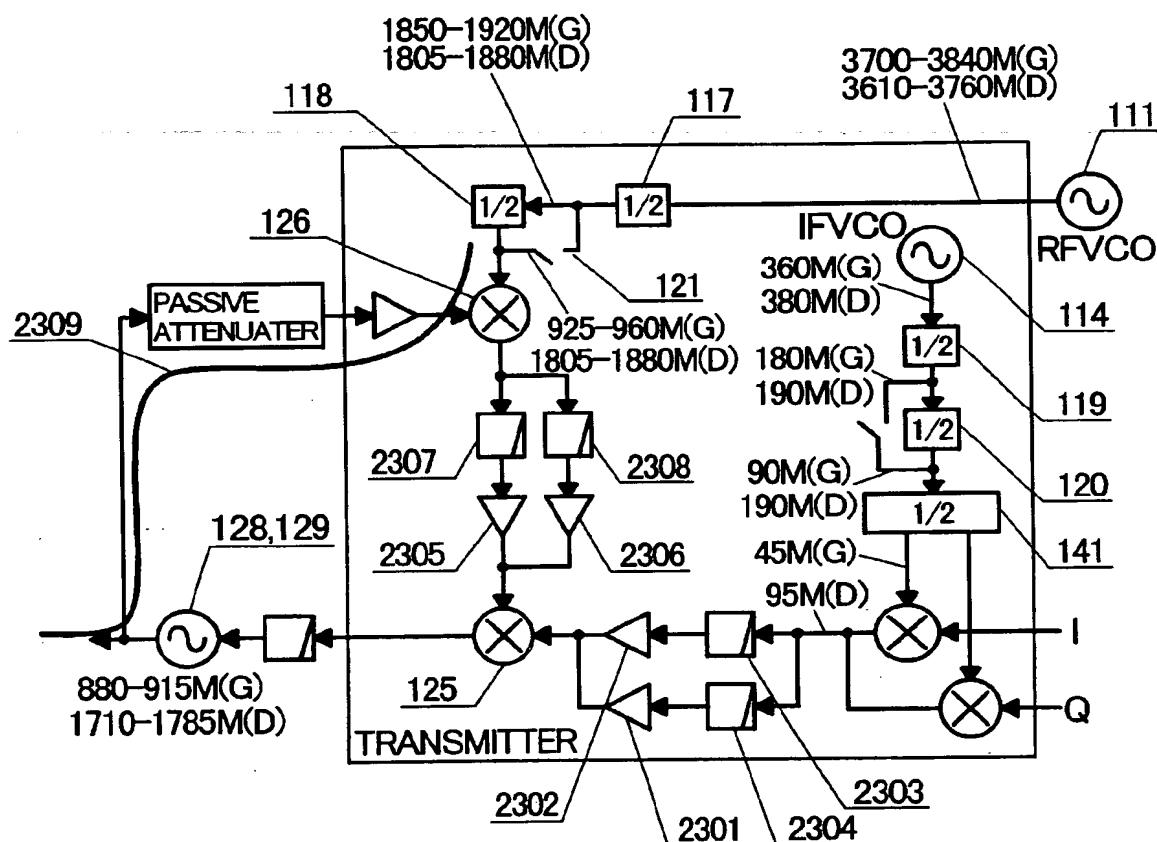
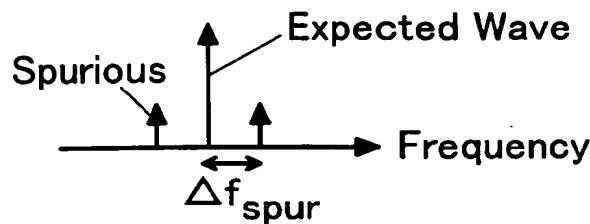


FIG.17



GSM Spurious

fIF [MHz]	42	44	45	46	46	48	50	52
m->	21	20	20	19	20	19	18	17
fVCO [MHz]								
880	2	0	20	6	40	32	20	4
882	0	2	18	8	38	30	18	2
884	2	4	16	10	36	28	16	0
886	4	6	14	12	34	26	14	2
888	6	8	12	14	32	24	12	4
890	8	10	10	16	30	22	10	6
892	10	12	8	18	28	20	8	8
894	12	14	6	20	26	18	6	10
896	14	16	4	22	24	16	4	12
898	16	18	2	24	22	14	2	14
900	18	20	0	26	20	12	0	16
902	20	22	2	28	18	10	2	18
904	22	24	4	30	16	8	4	20
906	24	26	6	32	14	6	6	22
908	26	28	8	34	12	4	8	24
910	28	30	10	36	10	2	10	26
912	30	32	12	38	8	0	12	28
914	32	34	14	40	6	2	14	30

FIG.18

DCS/1800 Spurious

f1F [MHz]	84	86	88	90	92	94	96	98	100	102	104	106
m->	21	20	20	19	19	19	18	18	17	17	17	16
fVCO [MHz]												
1710	54	10	50	0	38	76	18	54	10	24	58	14
1714	50	6	46	4	34	72	14	50	14	20	54	18
1718	46	2	42	8	30	68	10	46	18	16	50	22
1722	42	2	38	12	26	64	6	42	22	12	46	26
1726	38	6	34	16	22	60	2	38	26	8	42	30
1730	34	10	30	20	18	56	2	34	30	4	38	34
1734	30	14	26	24	14	52	6	30	34	0	34	38
1738	26	18	22	28	10	48	10	26	38	4	30	42
1742	22	22	18	32	6	44	14	22	42	8	26	46
1746	18	26	14	36	2	40	18	18	46	12	22	50
1750	14	30	10	40	2	36	22	14	50	16	18	54
1754	10	34	6	44	6	32	26	10	54	20	14	58
1758	6	38	2	48	10	28	30	6	58	24	10	62
1762	2	42	2	52	14	24	34	2	62	28	6	66
1766	2	46	6	56	18	20	38	2	66	32	2	70
1770	6	50	10	60	22	16	42	6	70	36	2	74
1774	10	54	14	64	26	12	46	10	74	40	6	78
1778	14	58	18	68	30	8	50	14	78	44	10	82
1782	18	62	22	72	34	4	54	18	82	48	14	86
1785	21	65	25	75	37	1	57	21	85	51	17	89

FIG.19

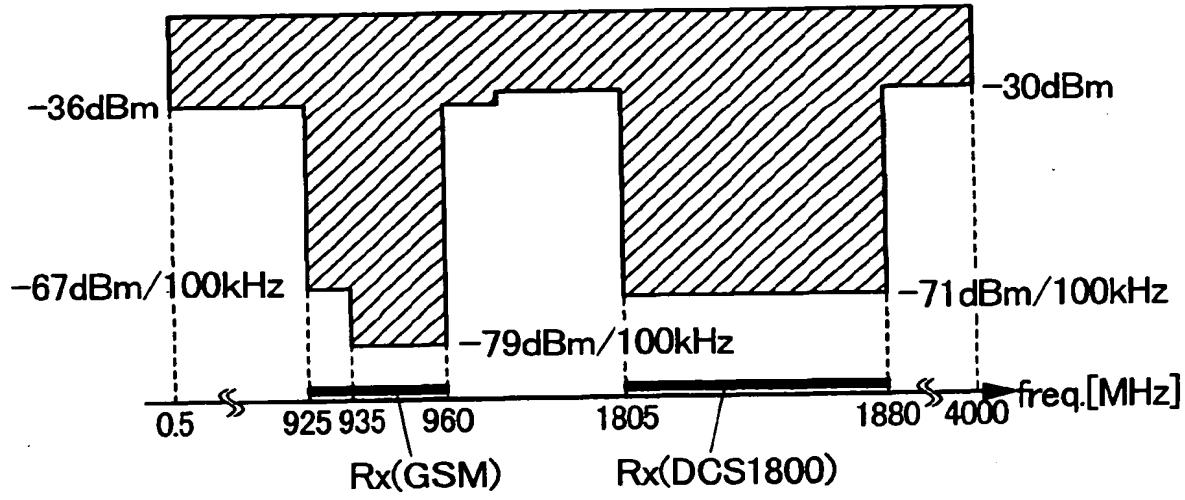
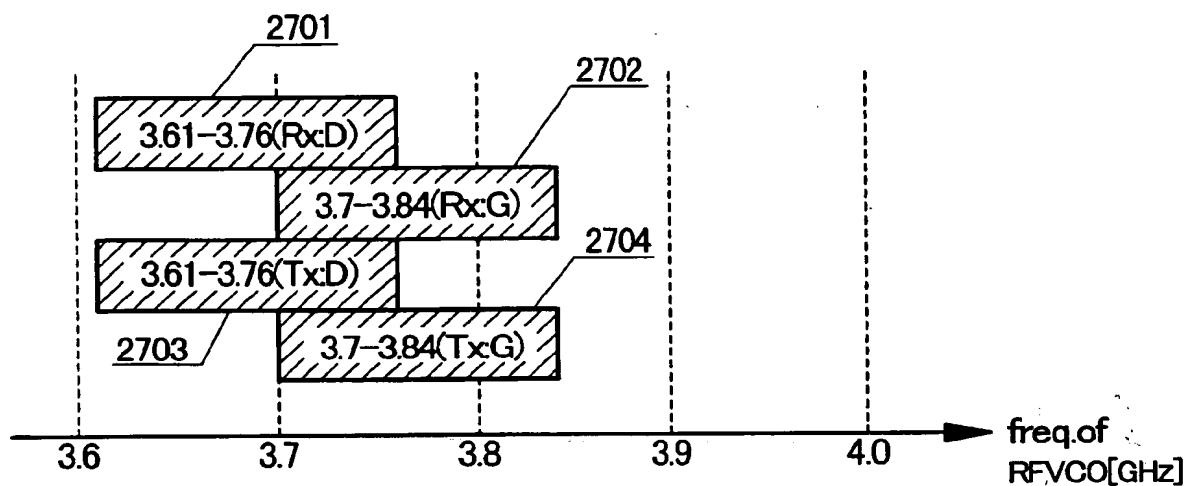
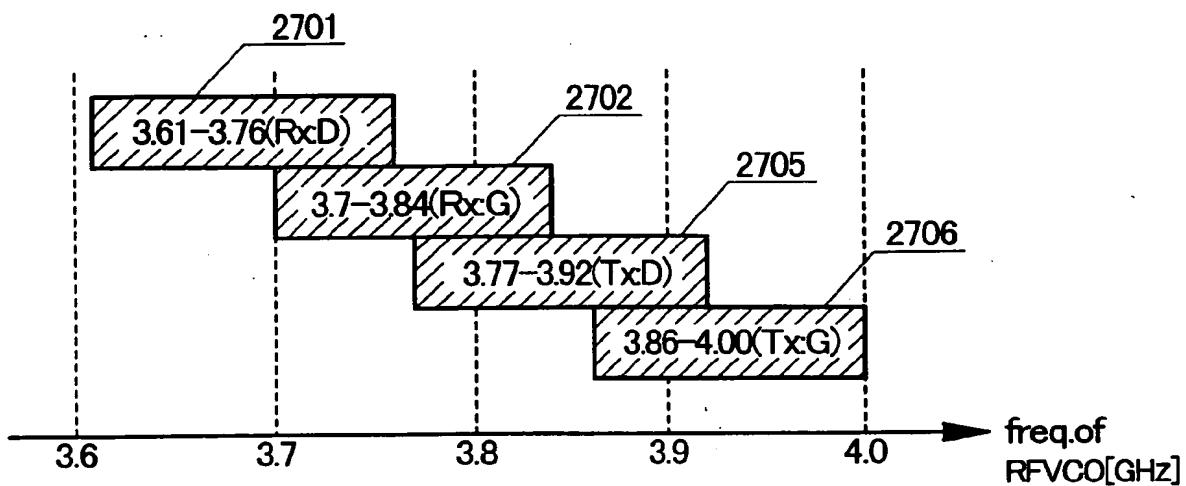


FIG.20



Total frequency range of RFVCO
= 3.61 – 3.84 GHz (230 MHz, 6.2%)

FIG.21



Total frequency range of RFVCO
= 3.61 – 4.00 GHz (390 MHz, 10.2%)